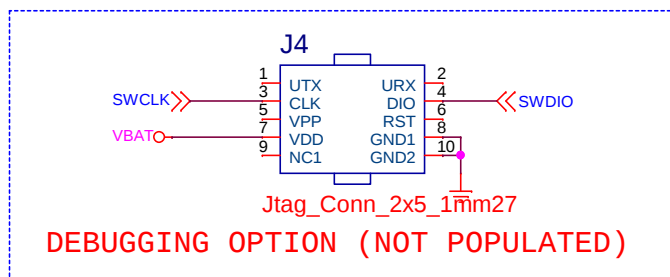


DA14531 Pro Development Kit

Design Name	d2632-db-wlcsp17_vE
Ref. Number	376-05-E
Version	E1.0
Date	Aug 8, 2019
Designer	PR
	D01 Version changes:KL E01 Version changes:KR

History Table		
Version	Date	Comments
A00	08 / Aug / 2018	Draft Release
	09 / Aug / 2018	Added option for hardware reset (P0_0 - R30) Added CIB debugging option (J4) Corrected mismatch in function notes (purple names) for MISO/SCLCK
A1.0	17 / Aug / 2018	Released to manufacturing
		Changed R1..R6 to 36 ohm Changed R23..R29 to N.P. Changed Y2 part number to SC20S-7PF20PPM (N.P.)
A1.1	29 / Nov / 2018	
A1.2	11 / Jan / 2019	Added Matching circuit Z1, Z3 • Z3 = 4.6nH / LQW15AN4N6B80D • Z1 = 1pF
A1.3	01 / Feb / 2019	BOM modifications for DCDC power optimization: • Changed L1 from BRL1608T2R2M to CBMF1608T2R2M • Changed C1, C2 from 10uF to 2.2uF
C1.0	28 / Feb / 2019	Changed L1 from CBMF1608T2R2M to DFE201610E-2R2M
D1.0	18/ Jul / 2019	Added placeholder for pi-shaped CLC filter (Z1, Z2, Z3) Added placeholder for decoupling capacitors: C6, C7 Changed RF matching components to : Z4, Z5 , Z6 Added resistors R34, R35 Changed C2 from 2.2uF to 10uF Added resistor R33 btw VBAT and VH+
E1.0	8/ Aug / 2019	Changed R15:360hm, pin-2 connection to SWDIO)from MB2_5 (J1B-pin B26) to P0_5 Changed R6 to not populated



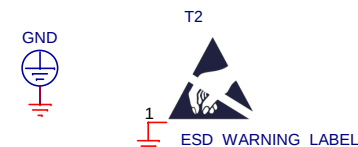
Configuration note

NOTE box

Changes in this Version.

TP11 FIDUCIAL

TP12 FIDUCIAL



<Variant Name>



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Title : DA14531/D2632 Development Kit Daughterboard			
Doc. Nr.	376-05-E	Designer: PR	Rev: E
Date:	Saturday, August 10, 2019	Sheet:	1 of 2

J1A

A1 A6
B9 B10
B10 B10
B13 B13
B13 B14
A24 A24
B28 B28
B30 B30
A10 A10
A10 A11
A11 A12
A12 A12
B32 B32
A14 A14
A15 A15
A16 A16
A17 A17
A18 A18
A19 A19
A20 A20
A21 A21
A22 A22
B1 B1
B1 B1
A25 A25
B20 B20
B16 B16
B16 B11
B11 B11
B31 B31
B24 B24
A31 A31
A32 A32

PCIE_64

VBAT
R33
NP
V+H
OVL+

J1B

B15 B15
A28 A28
B3 B3
B3 B18
B18 B22
B22 B22
B19 B19
A27 A27
B26 B26
B26 B26
B4 B4
B5 B5
B6 B6
B7 B7
A7 A7
A8 A8
A9 A9
B25 B25
A26 A26
B27 B27
A29 A29
A4 A4
B8 B8
A13 A13
A23 A23
B23 B23
B23 B29
B29 B29
A30 A30
B3 B3
A2 A2
A3 A3
B21 B21

PCIE_64

VBAT
TP1
RESET
SWCLK
SWDIO
MB0_0
MB0_3
MB0_4
MB0_5
MB0_6
MB0_7
MB2_0
MB2_1
MB2_2
MB2_3
MB2_4
MB2_5

